JEDEC STANDARD

A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress

JESD60A

(Revision of JESD60)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS

CONTENTS

Introduction

Hot-carrier-induced change of MOSFET parameters over time is an important reliability concern in modern microcircuits. High-energy carriers, also called hot carriers, are generated in the MOSFET by the large channel electric fields near the drain region. These hot carriers transfer energy to the lattice through phonon emission and break bonds at the Si/SiO_2 interface. The electric fields accelerate locally the carriers to effective temperatures well above the lattice temperature. Carriers also are injected into the SiO_2 and can be trapped there. The trapping or bond breaking creates oxide charge and interface traps that affect the channel carrier mobility and the effective channel potential.

In this document we will describe a procedure to characterize the hot-carrier-induced degradation of P-MOSFETs during channel conduction (i.e., $V_{GS} < 0$ V, $V_{DS} < 0$ V). In the case of p-channel devices, electrons, generated by impact ionization, can be trapped in the gate oxide near the drain region where the channel electric fields are maximum. These trapped electrons attract positive charge to the oxide interface and shorten the effective channel length. Depending on the device sensitivity to short channel effects, the electron-trapping enhances the p-channel MOSFET drive current, increases the channel mobility and transconductance, and decreases the absolute magnitude of the threshold voltage with consequent increase in off-state current.

In advanced submicron CMOS technologies (gate length < 0.25 μm, gate oxide thickness < 20-30 Angstroms), the p-channel devices' hot-carrier-induced damage has been observed to be dominated by hot-hole injection . This hot carrier degradation mechanism results in interface-state generation as well as positive fixed charge formation. P-MOSFET devices stressed under the hot-hole injection exhibit decreased p-channel MOSFET drive current, decreased channel mobility and transconductance, and increased absolute magnitude of the threshold voltage.

Both electron and hole injection can be a problem depending on the device operation in the circuit. The physical damage mechanism depends on the oxide thickness, vertical and channel electric field as well as the injection conditions.

Oxide (both positive and negative) charge and interface traps affect transistor performance in all operating regimes. Parameters such as threshold voltage, input and output transconductance, and drive currents are commonly monitored to identify performance change. The rate of change of each parameter is determined by the MOSFET design and IC process details. Both p- and n-channel MOSFETs are affected by hot carriers. This document addresses only p-channel MOSFETs that are operating with a conducting channel.

A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS

(From JEDEC Board Ballot JCB-04-46, formulated under the cognizance of the JC-14.2.2 Subcommittee on Device Reliability Working Group

1 Scope

The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process.

In this document, change criteria are specified. However, these are to be used for comparison purposes only and should not be used as acceptance or rejection criteria. It is also important to realize that this procedure should not be interpreted as a means of predicting MOS IC failure rates. The impact of the p-channel MOSFET change on actual circuit performance is not addressed in this document. Though this procedure was developed for wafer level stressing, it is also applicable to packaged structures.

The material contained in this publication was formulated under the cognizance of the JEDEC 14.2 Committee.

This document replaces JESD60 “A Procedure for Measuring p-channel MOSFET Hot-Carrier-Induced Degradation at Maximum Gate Current Under DC Stress.”

2 Applicable standards

ASTM F616-86, *Standard Method for Measuring MOSFET Drain Leakage Current*.

ASTM F617-86, *Standard Method for Measuring MOSFET Linear Threshold Voltage*.

ASTM F1096-87, *Standard Method for Measuring MOSFET Saturated Threshold Voltage*.

JESD77-B, *Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices*.

JESD28-1, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier Induced Degradation Under DC Stress.*

3 Terms and definitions

3.1 bulk current, dc (I_B): The direct current into the bulk contact.

3.2 bulk-source voltage (V_{BS}): The bulk-to-source voltage.

3.3 constant-current threshold voltage ($V_{T(ci)}$): The gate-source voltage at which the drain current is equal to a constant current, appropriate for a given P-MOSFET technology, times the ratio of gate width (W) to gate length (L). $V_{T(ci)}$ can be calculated using

$$\mathbf{V_{T(ci)} = V_{GS}\left(at\ I_D = I_{Do} \cdot \frac{W}{L} \right)} \quad (1)$$

where: W and L are the gate width and gate length as printed on the wafer;

I_{Do} is typically –0.025 μA but another value may be selected for a given technology such that

$V_{T(ci)}$ is in the subthreshold region of the device.

NOTE 1 The measurement technique must determine $V_{T(ci)}$ to within a 1-mV resolution. If the V_{GS} step size is larger than 1 mV, then a linear interpolation method may be used to achieve the 1-mV resolution.

NOTE 2 Typical dc bias voltages for the linear $V_{T(ci)}$ measurements are $V_{DS} = V_{DS(lin)}$ and $V_{BS} = V_{BB}$. For the saturation $V_{T(ci)}$ the measurements conditions are $V_{DS} = -V_{DD}$ and $V_{BS} = V_{BB}$. V_{DD} is the voltage at the external V_{DD} terminal and asuumed to be positive.

3.4 drain current, dc (I_D): The direct current into the drain contact.

3.5 drain leakage current ($I_{D(leak)}$): The drain current when the transistor is biased in its off state.

NOTE 1 $I_{D(leak)}$ may have contributions from channel off-state current, gate-induced drain leakage (GIDL), and drain-to-gate tunneling currents.

NOTE 2 Typical bias voltages for $I_{D(leak)}$ measurements are $V_{DS} = -V_{DD}$ and $V_{BS} = V_{GS} = V_{BB}$. V_{DD} is the voltage at the external V_{DD} terminal and asuumed to be positive.

3.6 drain-source voltage (V_{DS}): The drain-to-source voltage.

3 Terms and definitions (cont'd)

3.7 extrapolated threshold voltage ($V_{T(ext)}$): The threshold voltage extrapolated from measurement of maximum slope ($g_{m(max)}$) of the I_D-V_{GS} curve, as described in ASTM F617-86. $V_{T(ext)}$ can be calculated using

$$V_{T(ext)} = V_{GS}(g_{m(max)}) - \frac{I_D(g_{m(max)})}{g_{m(max)}} \quad (2)$$

where: $V_{GS}(g_{m(max)})$ is the gate voltage at the point of the maximum slope of the I_D-V_{GS} curve;

$I_D(g_{m(max)})$ is the drain current at the point of the maximum slope of the I_D-V_{GS} curve;

$g_{m(max)}$ is the maximum slope of the I_D-V_{GS} curve in the linear region.

NOTE The bias voltages for $V_{T(ext)}$ measurements are $V_{DS} = V_{DS(lin)}$ and $V_{BS} = V_{BB}$.

3.8 gate current, dc (I_G): The direct current into the gate contact.

3.9 gate-source voltage (V_{GS}): The gate-to-source voltage.

3.10 linear drain current ($I_{D(lin)}$): The drain current when the transistor is biased in the linear region.

NOTE Typical bias voltages for $I_{D(lin)}$ measurements are $V_{DS(lin)} = -0.1$ V, $V_{GS} = -V_{DD}$, and $V_{BS} = V_{BB}$. V_{DD} is the voltage at the external V_{DD} terminal and asuumed to be positive.

3.11 linear drain voltage ($V_{DS(lin)}$): The drain-to-source voltage for linear region measurements.

NOTE Typically, $V_{DS(lin)} = -0.1$ V.

3.12 maximum linear transconductance ($g_{m(max)}$): The maximum slope of the I_D-V_{GS} curve in the linear region.

NOTE 1 The gate voltage shall be varied in increments no greater than 20 mV from below the turn-on voltage to a value great enough to ensure that the maximum slope point has been reached.

NOTE 2 The slope shall be calculated using a three-point linear least-squares best-fit algorithm as defined in ASTM F617-86.

NOTE 3 Typical bias voltages for $g_{m(max)}$ measurements are $V_{DS} = V_{DS(lin)}$ and $V_{BS} = V_{BB}$.

3 Terms and definitions (cont'd)

3.13 metal-oxide-semiconductor field-effect transistor (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material; the gate is metal or another highly conductive material.

NOTE See JESD77-B for further clarification of MOSFET terms.

3.14 nominal bulk supply voltage (V_{BB}): The nominal bulk voltage for a given technology.

NOTE Typical $V_{BB} = 0$. If V_{BB} is not equal to zero, then V_{BB} for a P-MOSFET is positive.

3.15 nominal power supply voltage (V_{DD}): The nominal supply voltage for a given technology.

NOTE V_{DD} is positive.

3.16 punch-through voltage (V_{PT}): The reverse-bias drain voltage applied to the drain terminal that results in significant drain-to-source current even though the transistor is biased in its off state.

NOTE 1 Punch-through is differentiated from junction breakdown in that the current path is from drain to source instead of from drain to substrate, as is the case of junction breakdown.

NOTE 2 Typical dc bias voltages for V_{PT} measurements on p-channel MOSFET devices are V_{DS} at $I_D = -1\ \mu A$ and $V_{GS} = V_{BS} = V_{BB}$.

3.17 saturation drain current ($I_{D(sat)}$): The drain current when the transistor is biased in the saturation region.

NOTE Typical bias voltages for $I_{D(sat)}$ measurements are $V_{DS} = V_{GS} = -V_{DD}$ and $V_{BS} = V_{BB}$. V_{DD} is the voltage at the external V_{DD} terminal and asuumed to be positive.

3.18 time to target (t_{tar}): The time it takes under specific conditions for the value of a particular parameter to change by a specified amount or to a specified value.

NOTE For most parameters, a change of 10% from the unstressed value is often used. For threshold voltage, a 50 mV change is often used. No criterion is specified for the drain leakage current. These values have been arbitrarily chosen, and no relationship to circuit failure is implied. Other criteria (e.g., 5% change from the unstressed value) may be used for a given technology.

4 Technical requirements

4.1 Equipment requirements

The measurement system must be capable of the simultaneous application of voltage and measurement of current at the gate, drain, and substrate contacts of the transistor. The system must be able to measure 100 pA with a resolution 1 pA or better. The voltage overshoot during parametric measurements and stress must not exceed 1% of the applied voltage. The measurement system must be capable of supplying the maximum stress current of the transistor.

4.2 Test structure requirements

A p-channel MOSFET fabricated on a n-type bulk substrate/well should be used. A minimum channel length of the process is recommended, but other channel lengths may also be used. Current drive should be small enough so that the stress does not raise the junction temperature more than 5 ^{o}C. The source, drain and gate contacts of the transistor must be contacted. The bulk shall be contacted or floating depending on the technology under inverstigation (e.g., silicon-on-insulator pMOSFETs can have floating n-wells). To minimize parasitic voltage drops between the applied drain stress voltage and the device, the resistance from the probe pads to the device source, drain, and substrate should be minimized. The pMOSFET devices must be designed to reduce possible charging effects and to have an antenna ratio at or below the design specification.

4.3 Measurement requirements

The device should be set up at the wafer level on a probe station providing a stable platform via a vacuum chuck or as a packaged part in a test fixture. Chuck or fixture temperature shall be set at the stress and test temperature of interest. Test temperature should be set based upon worst case hot carrier effect of the particular process technology. This may be highly dependent upon operating bias regime of the technology. Once set, this temperature must be maintained to within +/- 2.0 °C of this set point for the duration of the test. The user should also report the test temperature.

At the end of each hot-carrier stress interval, the stress is terminated and device parameters are measured. The stress time interval should be known to an accuracy of +/- 1% for stress time intervals over 1 second and 10% for stress intervals less than 1 second.

5 Hot-carrier stress test procedures

Figure 1 describes the hot-carrier stress test procedure.

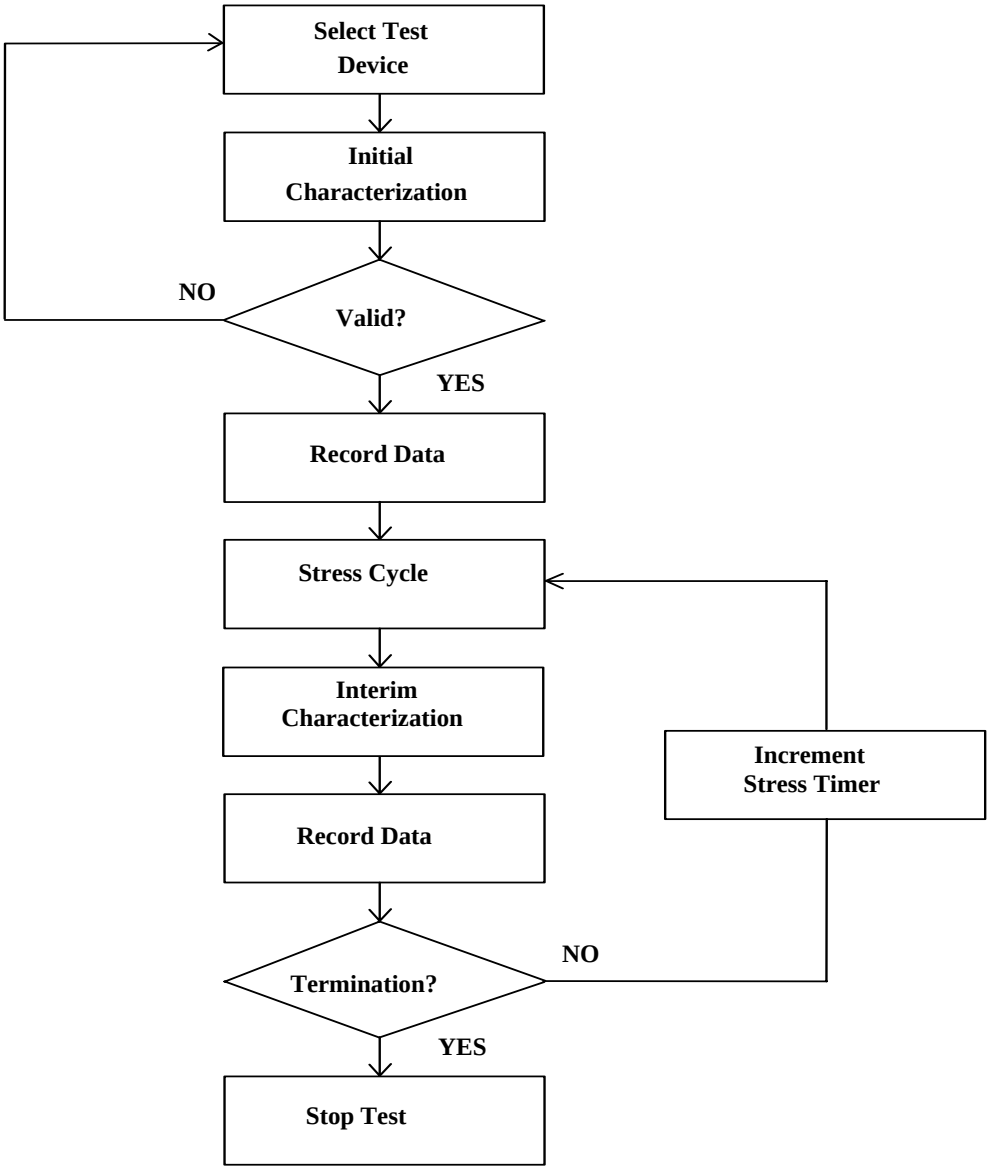

Figure 1 — Hot-carrier stress test procedure

5 Hot-carrier stress test procedures (cont'd)

Initial tests are used to select a "good" device (see 5.2) and to determine initial unstressed parameter values. If the device is determined to be "good," data is recorded and the stress cycle begins. During the stress cycle the device is biased using the selected stress bias condition. Since changes in parameters typically exhibit a logarithmic behavior the recommended stress intervals are at least 1/2 decade time-steps (see 5.4). After each stress cycle the device parameters are again determined, recorded and compared to the initial values. If the parameter degradation exceeds the termination criteria (see 5.6), testing ends. Otherwise, another stress cycle is initiated. The sections below describe in greater detail the hot-carrier stress algorithm.

5.1 Determining stress bias conditions

Hot-carrier stressing should be performed under constant voltage bias conditions at the temperature specified in 4.3.

To determine the maximum drain stress voltage, the I_D-V_{DS} curves for the device must be examined. Examples of I_D-V_{DS} characteristic curves for a p-channel MOSFET are shown in Figure 2. Here, The drain current is plotted as a function of drain voltage at three different gate bias conditions.

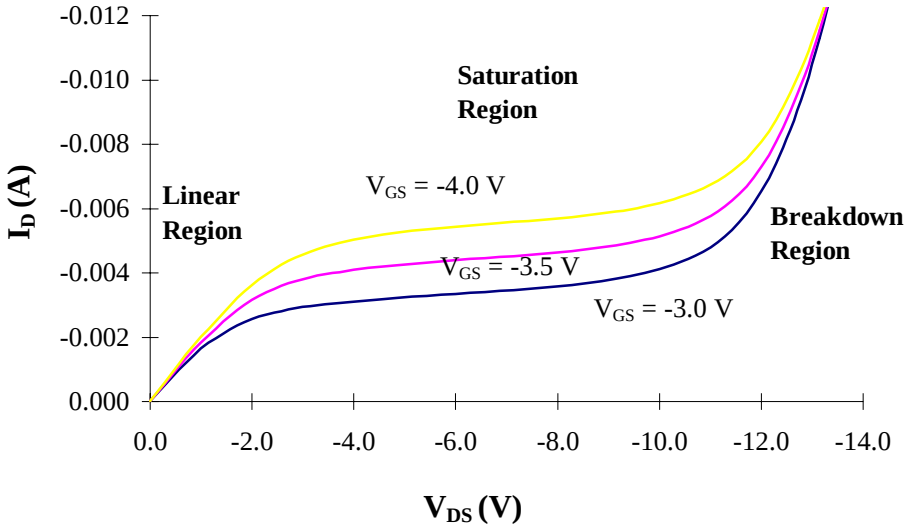

Figure 2 — P-channel MOSFET drain current characteristics

5 Hot-carrier stress test procedures (cont'd)

5.1 Determining stress bias conditions (cont'd)

The linear, saturation, and breakdown regions are shown on the plot. Transistor breakdown, whether due to drain avalanching, punch-through, or bipolar snapback determines the maximum V_{DS} stress limit at a given V_{GS}, V_{BS} conditions and temperature. Special care should be take not to stress in this region without checking the linearity of the acceleration. It is recommended to limit maximum drain stress bias voltage to less than 80% of actual breakdown. This test should be performed at the stressing conditions of interest. This will ensure realistic channel hot-carrier conditions and reduce the possibility for catastrophic failure during stress. The minimum realistic drain stress bias is restricted by long test times or by inaccurate extrapolations to t_{TAR}.

For technologies where the peak I_G results in the worst hot-carrier degradation are representative of the use scenario, the gate bias should be set to induce the maximum possible gate current. This typically occurs when V_{GS} is approximately $1.1V_t$ to $1.5V_t$. Although peak I_G gate biasing may produce the greatest rate of p-channel MOSFET change in some technologies (e.g., buried-channel P-MOSFETs in DRAM technologies), this must be verified for the technology under test. An example I_G-V_{GS} plot is shown in Figure 3. For this device, a gate-bias ramp voltage was applied with the drain voltage set at the selected stress V_{DS}.

For p-channel devices (gate length below 0.25 μm), the worst-case bias conditions may be V_{GS}=V_{DS} (maximum hole injection condition).

It is possible that for a given technology or device that neither V_{GS} at peak I_G or V_{DS} = V_{GS} will induce maximum possible PMOS degradation behavior. In these cases, the V_{GS} that produces worst case degradation for the use scenario should be determined empirically. The user should perform measurments to determine which gate voltage produces the greatest rate of degradation. The gate voltage at peak degradation should be established with a series of hot-carrier tests at a fixed V_{DS} with a minimum of 5 different V_{GS} values that span the expected gate use voltage of the device.

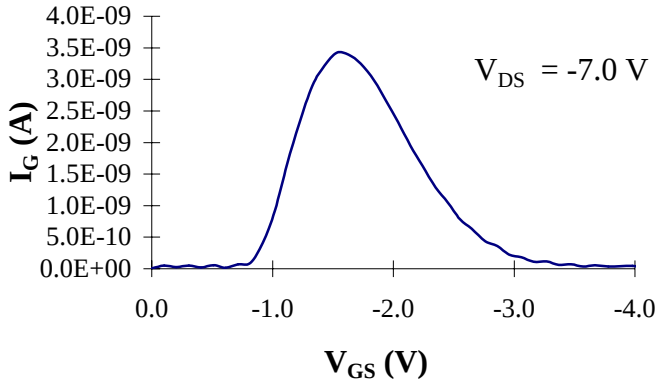

Figure 3 — P-channel MOSFET gate current characteristics

5 Hot-carrier stress test procedures (cont'd)

5.2 Test devices

A transistor with gate, drain, and source leakage currents that meet the requirements of the process shall be used. Transistors used for determing peak damage stressing condition, for source-to-drain breakdown measurements, or for any other test that use bias voltages greater than nominal operating conditions shall not be used for hot-carrier stress testing.

5.3 Initial characterization

Monitored parameters shall include $V_{T(ci)}$, $V_{T(ext)}$, $g_{m(max)}$, $I_{D(lin)}$, $I_{D(leak)}$ and $I_{D(sat)}$ all in the forward and reverse mode unless the device is operated in forward mode only. The parameters shall be recorded, as these will be used for determining parametric shifts. Other parameters may also be measured such as gate leakage at operating voltage, breakdown, punch through voltage (V_{PT}), etc. Measurements are done at stress temperature.

NOTE A forward-mode measurement is made with the drain and source terminals at the same bias configuration as during the stress. A reverse-mode measurement is made with the drain and source terminals switched from their stressing configuration.

5.4 Stress cycle

The transistor will be stressed with the voltages determined in 5.1. The voltages shall be applied in the following order: V_{BS} first, V_{GS} second, and V_{DS} last. The stress begins when V_{DS} has been applied. The stress continues until the stress time interval has been completed. Turning off the bias shall be done in the reverse order, with V_{DS} first, V_{GS} second, and V_{BS} last.

Since the typical degradation follows a logarithmic function with time, the recommended stress intervals are 1/2 decade time-steps. For example, the cumulative stress times could be 10, 30, 100, 300, 1000, 3000, 10000, 30000, and 100000 seconds. In this example, the device would be stressed for 10 seconds. After this stress interval, the device parameters are measured. The device would then be stressed for 20 additional seconds and the parameters again measured. The next stress interval would be 70 seconds. This procedure continues until stress termination occurs.

5.5 Interim characterization

The six parameters that shall be measured and recorded are $V_{T(ci)}$, $V_{T(ext)}$, $g_{m(max)}$, $I_{D(lin)}$, $I_{D(leak)}$ and $I_{D(sat)}$. Other parameters may also be measured. Measurements are done at stress temperature.

5 Hot-carrier stress test procedures (cont'd)

5.6 Stress termination

Each device shall be stressed until at least the worst-case parameter reaches or exceeds t_{TAR} or two time decades of valid data have been taken (see 7.4).

6 Data analysis

Percent change for $g_{m(max)}$, $I_{D(sat)}$, $I_{D(leak)}$ and $I_{D(lin)}$ is calculated from:

$$\mathbf{Y(t) = \frac{P(t) - P(0)}{P(0)} * 100} \quad (3)$$

where: P(0) is the initial parameter value.

P(t) is the parameter value at time t.

Relative shift for $V_{T(ci)}$ and $V_{T(ext)}$ is calculated from:

$$\mathbf{Y(t) = P(t) - P(0)} \quad (4)$$

For devices stressed at peak I_G, the parameter change may fit the following equation using a least-squares fit:

$$\mathbf{|Y(t)| = CLog(t)} \quad (5a)$$

where: $|Y(t)|$ is the absolute or percent change value change in the parameter.
t is the cumulative stress time.

For devices which are dominated by interface-state damage, the parameter change may follow the following equation using a least-squares fit:

$$\mathbf{|Y(t)| = Ct^n} \quad (5b)$$

where: $|Y(t)|$ is the absolute value or the percent change in the parameter.

t is the cumulative stress time.

For Equation 5a and 5b you should verify the time dependence for your technology and stress condition and use the applicable time model.

6 Data analysis (cont'd)

For each parameter analyzed, t_{TAR} should be interpolated or extrapolated from the data based on the C value from this least-squares fit. Figure 4 shows an example of the use of Equation 5a. See applicable precautionary notes in 7.3 and 7.4.

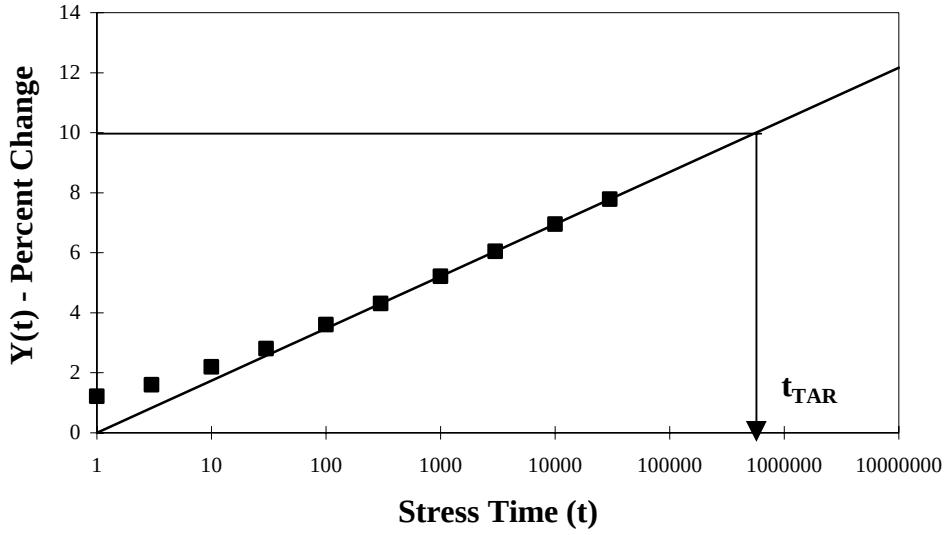

Figure 4 — Example of Logarithmic Fit to Hot-carrier Stress Data

7 Precautions

While the procedures outlined above are quite straightforward, there are subtle effects that can cause significant errors. Listed below are some precautions that shall be followed to ensure correct implementation of the procedure.

7.1 Test Sample

It is essential that devices used in hot-carrier stress testing should be unstressed devices. Test devices should not have been operated at a bias condition exceeding the nominal power supply voltage of the technology. Pre-stressed devices can show an appreciable shift in t_{TAR} when compared to unstressed parts. The optimal gate stress bias voltage must be determined from identically processed but different devices than those to be hot-carrier stress tested.

7 Precautions (cont'd)

7.2 Stress

Since the change in parameters are a sensitive exponential function of applied stress voltage, it is essential that the correct stress bias voltage be applied to the device under test. Discrepancies can arise due to high series resistance caused by poor probe-to-pad contact or from device short circuits leading to power supply compliance limitations. It must be determined that the MOSFET gate has not short-circuited during the stress. This is particularly true for p-channel MOSFET devices where oxide electron traps are the driving force behind the parameter changes.

7.3 Interim measurements

Certain technologies have shown partial parameter recovery once stress biasing is removed. In this case, parameter measurements should be made as soon as possible after each stress cycle has been completed, and additional stressing restarted immediately.

Significant device self-heating may occur during stress testing. This effect may be more pronounced in packaged test transistors. On parts that exhibit significant device heating measurements should begin when the device temperature reaches within 1 C^o of the original measurement temperature.

When a device degradation parameter reaches its specified stress termination criteria, it may be worth continuing the stress beyond t_{TAR}. This ensures a good interpolation of data around t_{TAR}, especially if the degradation data is noisy.

7.4 Data analysis

Data measurements that are outside the range of the equipment resolution should not be included in the analysis.

8 Required reporting

As a minimum, the following information relevant to the p-channel MOSFET hot-carrier measurement should be reported.

8.1 Test transistor identification

Provide information sufficient to uniquely identify the MOSFET tested.

- Gate oxide thickness and process, Source/Drain Engineering, etc.
- Lot, Wafer and chip location.

8 Required reporting (cont'd)

8.2 V_{DD}, V_{BB}

The nominal power supply and bulk voltage for the process technology.

8.3 MOSFET channel length and width

The final gate dimensions as printed on the wafer for the p-channel MOSFET under test. In addition the effective channel length, as measured by an adequate extraction method, should be reported.

8.4 V_{DS} at stress, V_{BS} at stress, V_{GS} at stress

The MOSFET drain, bulk and gate voltage applied during stress.

8.5 Initial I_G and I_B and I_D at stress

The initial MOSFET gate and bulk and drain current at stress conditions.

8.6 Initial $I_{D(lin)}$, $g_{m(max)}$, $V_{T(ci)}$, $V_{T(ext)}$, $I_{D(sat)}$, $I_{D(leak)}$

The initial (pre-stress) characterization data.

8.7 t_{TAR} for $I_{D(lin)}$, $g_{m(max)}$, $V_{T(ci)}$, $V_{T(ext)}$, $I_{D(sat)}$, $I_{D(leak)}$

The calculated Time to Target (see 3.18) for each of the six required parameters (if possible). A plot of the time model used to fit the degradation model should be provided.

8.8 Total test time

The total cumulative stress time.

8.9 Measurement temperature

The chuck or fixture temperature maintained during the measurement (3.3).

8.10 Linear drain voltage $V_{DS(lin)}$

The dc drain-to-source voltage for linear region measurements (see 3.11).

Annex A (informative) Differences between JESD60A and JESD60

This table briefly describes most of the changes made to entries that appear in this standard, JESD60A, compared to its predecessor, JESD60 (April 1997). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Term and description of change
iii	**Title:** Changed title to remove words "AT M AXIMUM GATE CURRENT."
iii	**Introduction:** Included new paragraph describing different degradation mechanism for advanced submicron P-Channel devices.
2	**Definitions:** Alphabetized definitions.
2	**constant-current threshold voltage:** Revised definition to improve clarity.
3	**maximum linear transconductance:** Revised definition to improve clarity.
4	**time-to-target:** Revised definition to improve clarity.
5	**Equipment Requirements:** Added sentence requiring measurement system to be capable of supplying maximum stress current of the transistor.
5	**Test Structure Requirements:** Added comment on bulk contact for situation of SOI.
5	**Test Structure Requirements:** Added comment that structure should be designed to minimize possible charging effects.
5	**Measurement Requirements:** Changed temperature maintenance requirement from +/-1^{o}C to +/-2^{o}C.
8	**Determining Stress Bias Conditions:** Changed maximum drain bias voltage from 90% to 80% of actual breakdown.
8	**Determining Stress Bias Conditions:** Added 3 paragraphs which discuss situations where worst-case bias may not be at maximum gate current as it is for classic technologies.
9	**Initial Characterization:** Added reverse-mode measurements to list of monitored parameters.
10	**Data Analysis:** Included power-law model for devices which are dominated by interface-state damange.
12	**Precautions, Data Analysis:** Removed paragraph covering modern technologies; material is already covered by earlier paragraphs in the new document.

Standard Improvement Form **JEDEC JESD60A**

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